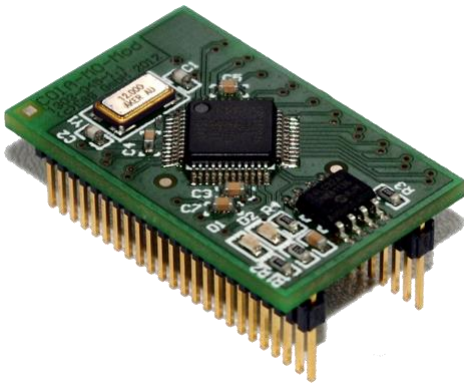


# CANopenIA-M0

## The second generation CANopenIA solution



The CANopenIA-M0 is the recent replacement for the CANopenIA-XA chip and module solutions. The chip implements the CANopen protocol compliant to the CiA standards

- CiA301 version 4.2 (CANopen application layer and communication profile),
- CiA305 version 2.2.14 (Layer setting services and protocols) and
- CiA401 version 3.0 (Device profile for generic I/O modules).

### Powerful Processor

CANopenIA-M0 is based on the NXP Cortex M0 32-bit micro controller. A derivative with integrated CAN transceiver is used to minimize the external components needed around the protocol chip. The Cortex architecture in conjunction with the optimized firmware design results in a very high performance. Time delays between in our outgoing CAN PDOs and hardware events are brought down to 15 micro seconds.

### Chip or Module

This high performant and ready to use CANopen solution is available as a chip or as a module. The module implements around the chip the clock generation, a serial EEPROM to store the configuration data and two LEDs to signal the CANopen state. To become familiar with COIA-M0 a starter kit is available.

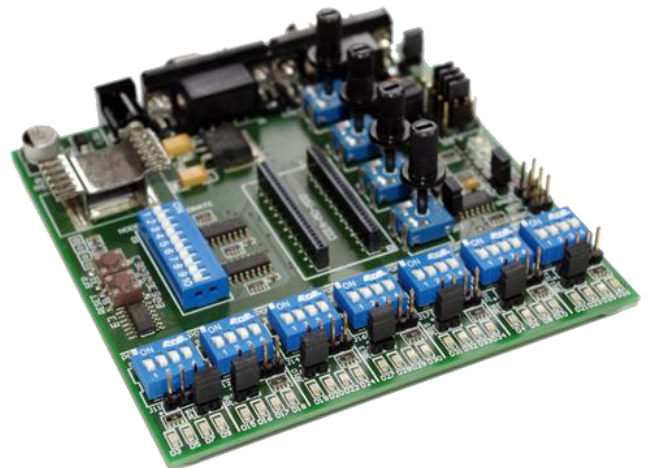
Entries in the object dictionary, the I/O ports and the SDO and PDO behavior is configured with a straightforward setup tool.

### Chip Features

- 48-pin LQFP package (9 x 9 mm<sup>2</sup>)
- Industrial temperature (-40 to 85 °C) range
- 12 MHz external oscillator leads to an internal operating frequency of 48 MHz
- I<sup>2</sup>C interface to connect the configuration EEPROM
- Two SPI interfaces to connect external D/A and A/D converters

### COIA-M0 CAN Features

- The fast and high-performant internal CAN controller works with 32 bit message objects and supports all CANopen data rates up to 1 Mbps
- CANopen protocol implemented in flash
- Up to four transmit process data objects (TPDO)
- Up to four receive process data objects (RPDO)
- Transmission types configurable by SDO access to object dictionary
- Fast response times down to 15 µs due to the architecture optimized CANopen implementation



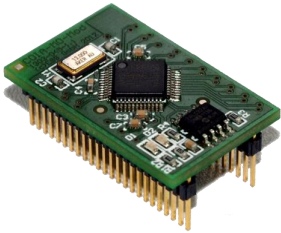
*The CANopenIA-M0 evaluation board*

# CANopenIA-M0

The second generation CANopenIA solution

## CANopenIA-M0 Module

The CANopenIA-M0 Module allows integration of the CANopenIA-M0 chip functions in user's hardware without taking care about clock generation, EEPROM hardware and the status and error indication. The module can easily be implemented in user's hardware with a two row 48 pin connector. Components can be placed under the module on the main PCB. The module includes the COIA-M0 chip, the clock generation, the EEPROM to store the setup data and two LEDs to signal status and error information according to the CANopen specification. The connector has 1.27mm grid with two rows of 24 pins each.



## CANopenIA-M0 Starter Kit

The CANopenIA-M0 starter kit contains all you need to immediately get a CANopen environment up and running:

- USB to CAN adapter with related software
- CANopenIA-M0 evaluation board with COIA-M0 module and product CD
- Wall power supply and all needed cables for wiring

## CANopenIA-M0 Evaluation Board

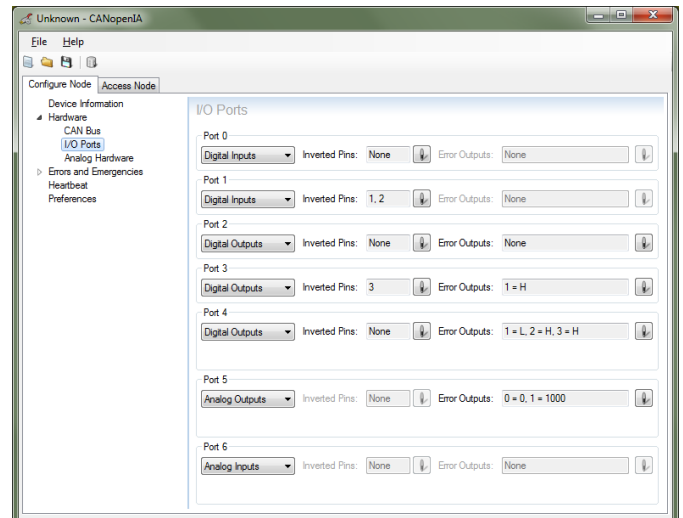
The evaluation board included in the COIA-M0 starter kit provides

- Two CAN connectors with a switchable terminating resistor
- DIP switches for setting baud rate and node ID
- 28 LEDs to signal the state of the binary output port pins
- 28 switches to stimulate the binary input port pins
- 4 Potentiometer to stimulate either the internal or the external ADC ports
- 4 LEDs to signal the output voltage on the external DAC ports

## COIA-M0 Setup Tool

With the CANopenIA-M0 Setup Tool all features supported by the CANopenIA-M0 chip are configured in a very easy manner.

The setup tool generates a data set to be downloaded to the chip and a device configuration file which can be read by third party CANopen bus configuration tools.



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